LISTING OF THE CLAIMS:

Claim 1 (Currently Amended) A memory structure comprising:

a transistor having an emitter, a base, and a collector, said base having a lower surface adjacent an insulating layer; and

a base contact comprising a phase change material liner, wherein a portion of said phase change material liner is located directly on a surface of said base.

Claim 2 (Currently Amended) The memory structure of Claim 1, wherein said transistor induces phase changes in said phase change material liner.

Claim 3 (Currently Amended) The memory structure of Claim 1, wherein said phase change material liner comprises a chalcogenide alloy.

Claim 4 (Original) The memory structure of Claim 3, wherein said chalcogenide alloy comprises $Ge_2Sb_2Te_5$.

Claim 5 (Cancelled)

Claim 6 (Currently Amended) The memory structure of Claim 1, wherein said emitter is n-type, said base is p-type, said collector is n-type and said base contact further includes a region of ~~is~~ p-type polysilicon.

Claim 7 (Currently Amended) The memory structure of Claim 1, wherein said emitter is p-type, said base is n-type, said collector is p-type and said base contact further comprises a region of ~~is~~ n-type polysilicon.

Claim 8 (Original) The memory structure of Claim 1, wherein said insulating layer comprises a buried oxide (BOX) layer of a silicon-on-insulator substrate.

Claim 9 (Original) A semiconductor structure comprising:

a substrate comprising a first doped region flanked by a set of second doped regions;

a phase change material positioned on said first doped region; and

a conductor positioned on said phase change material, wherein when said phase change material comprises a first phase said semiconductor structure operates as a bipolar junction transistor, and when said phase change material comprises a second phase said semiconductor structure operates as a field effect transistor.

Claim 10 (Original) The semiconductor structure of Claim 9, wherein said phase change material comprises a chalcogenide alloy.

Claim 11 (Original) The semiconductor structure of Claim 10, wherein said chalcogenide alloy comprises $Ge_2Sb_2Te_5$.

Claim 12 (Original) The semiconductor structure of Claim 9,wherein said first phase comprises a crystalline solid phase.

Claim 13 (Original) The semiconductor structure of Claim 9, wherein said second phase comprises an amorphous solid phase.

Claim 14 (Original) The semiconductor structure of Claim 9, wherein said phase change material is converted to said first phase or said second phase by heat radiating from said substrate.

Claim 15 (Original) A method of forming a memory device comprising:

providing an initial structure comprising a sacrificial gate atop a first conductivity region in a Si-containing layer of an SOI substrate, said sacrificial gate flanked by a set of spacers;

forming second conductivity regions abutting said first conductivity region in said Si-containing layer;

removing said sacrificial gate to provide a gate via;

forming a phase change material liner within at least a portion of said gate via; and

forming a gate conductor on said phase change material liner.

Claim 16 (Original) The method of Claim 15, wherein said phase change material liner comprises a chalcogenide alloy.

Claim 17 (Original) The method of Claim 15, wherein said phase change material liner has a thickness of less than about 20 nm.

Claim 18 (Original) The method of Claim 15 wherein said sacrificial gate comprises polysilicon.

Claim 19 (Original) The method of Claim 18 wherein said removing said sacrificial gate comprises etching said sacrificial gate with KOH.

Claim 20 (Original) The method of Claim 15 wherein forming said phase change material liner comprises sputtering or chemical vapor deposition (CVD) at temperatures less than about 600°C.